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Control Structure, FSM

* Control structure = representation of steps that need to be executed within the lc3 in order to perform some task?

Assembly

* Decimal: #
* Binary: b
* Hex: x

Quiz notes:

* PC: takes input from a MUX that chooses between:
  + PC + 1
  + Content of some base register (SR1OUT)
* ALU: can add/complement/and between outputs:
  + 1st is from specified base register
  + 2nd is either from imm5 or another base register
* Memory:
  + MAR holds address of a memory location
  + MDR stores contents of a memory location on its way to/from storage
* FETCH: 3 steps

1. MAR loaded w/ contents of PC while the PC is simultaneously incremented
2. Memory interrogated at address specified by MAR and loaded into MDR        (MDR <- M[MAR])
3. Contents of MDR loaded onto IR

* Other steps:
  + DECODE: using FSM
  + EVAL ADDRESS: computes address of memory location that needs to be accessed
  + FETCH OPERANDS: fetches whatever is needed from either memory or registers (ex. In LDR, an address is computed by adding base + offset (eval address), and then the data in M[base + offset] is fetched from memory loaded into the DR)
  + EXECUTE, STORE RESULT